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10/576,246	09/27/2006	Henning Sirringhaus	Q94482	8834

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EXAMINER	
LEE, JAE	

ART UNIT	PAPER NUMBER
2895	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/576,246	SIRRINGHAUS ET AL.	
	Examiner	Art Unit	
	JAE LEE	2895	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 and 3-34* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1, 3-34* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Applicant's arguments filed 07/21/2008 have been fully considered but they are not persuasive.

Applicant contends of an inevitable result that a bit of the semiconductor layer 23 is etched along with the contact layer **25** and that no teaching of the prior art of record provides no positive effect of such a recess. Examiner disagrees and submits that a function of the inevitable recess formed is irrelevant to such claim language and the prior art, namely Gu et al., clearly provides a structure with a channel length that is greater than the actual physical distance of the source and drain electrodes (see Fig. 6). Regardless of the positive or negative impact of the recess, the prior art clearly discloses the recess and is sufficient in reading claim 1.

Claim Objections

2. **Claims 29, 31, and 32** objected to because of the following informalities:

   a. Numbering of **claims 31 and 32** are incorrect, cancelled **claims 31,32** existed in previous amendments.

   b. "preferably" is unclear to the examiner as to whether or not the insulating material is REQUIRED to deposit between source and drain, but not on top of source-drain electrodes.

3. Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. **Claims 31-34** are rejected under 35 U.S.C. 102(b) as being anticipated by Chan (USP# 5,407,846, hereinafter Chan).

With regards to **claim 31**, Gu et al. teaches a thin film transistor electronic switching device, comprising:

a source electrode and a drain electrode (see Fig. 4, source **8a**. drain **8b**);

a semiconducting region in contact with and extending between the source and drain electrodes (see Fig. 4, semiconducting region **6**);

a gate electrode disposed for influencing the transconductance of at least part of the semiconducting region (see Fig. 4, gate electrode **6a**, inherent that the gate electrode will influence transconductance since drain current and the gate electrode voltage will change during operation of the device); and

an insulating region located between the source and drain electrodes and configured so that the length of the shortest current path through the semiconducting region between the source and drain electrodes is greater than the shortest physical distance between the source and drain electrodes for the purpose of spsuppressing the off-current of the electronic switching device (see Fig. 4, insulating region **5**, current path between source **8a** and drain **8b** must be larger than the physical separation

distance between source **8a** and drain **8b**, same structure claimed will have same result).

With regards to **claim 32**, Gu et al. teaches a thin film transistor electronic switching device, comprising:

a source electrode and a drain electrode (see Fig. 4, source **8a**. drain **8b**);

a semiconducting region in contact with and extending between the source and drain electrodes (see Fig. 4, semiconducting region **6**);

a gate electrode disposed for influencing the transconductance of at least part of the semiconducting region (see Fig. 4, gate electrode **6a**, inherent that the gate electrode will influence transconductance since drain current and the gate electrode voltage will change during operation of the device); and

an insulating region located between the source and drain electrodes and configured so that the length of the shortest current path through the semiconducting region between the source and drain electrodes is greater than the shortest physical distance between the source and drain electrodes (see Fig. 4, insulating region **5**, current path between source **8a** and drain **8b** must be larger than the physical separation distance between source **8a** and drain **8b**).

wherein the shortest current path through the semiconductor region between the source and drain electrodes is defined other than by etching the semiconductor region between the source and drain electrodes (see Fig. 4, no etching performed).

With regards to **claim 33**, Chan teaches a method for forming a thin film transistor electronic switching device, the method comprising:

forming a source electrode and a drain electrode (see Fig. 1a, source **31** and drain **29**);

forming a semiconducting region in contact with and extending between the source and drain electrodes (see Fig. 6, semiconductor layer **23**);

forming a gate electrode disposed for influencing the transconductance of at least part of the semiconducting region (see Fig. 6, gate electrode **17**, inherent that the gate electrode will influence transconductance since drain current and the gate electrode voltage will change during operation of the device, $g_m = dI / dE$, where dI = change in drain current and dE = change in gate voltage); and

forming an insulating region located between the source and drain electrodes and configured so that the length of the shortest current path through the semiconducting region between the source and drain electrodes exceeds the shortest physical distance between the source and drain electrodes for purpose of suppressing the off-current of the electronic switching device (see Fig. 6, insulating region **33**, current path between source **31** and drain **29** must be larger than the physical separation distance between source **31** and drain **29**, same structure claimed will have same result).

With regards to **claim 34**, Chan teaches a method for forming a thin film transistor electronic switching device, the method comprising:

forming a source electrode and a drain electrode (see Fig. 1a, source **31** and drain **29**);

forming a semiconducting region in contact with and extending between the source and drain electrodes (see Fig. 6, semiconductor layer **23**);

forming a gate electrode disposed for influencing the transconductance of at least part of the semiconducting region (see Fig. 6, gate electrode **17**, inherent that the gate electrode will influence transconductance since drain current and the gate electrode voltage will change during operation of the device, $g_m = dI / dE$, where dI = change in drain current and dE = change in gate voltage); and

forming an insulating region located between the source and drain electrodes and configured so that the length of the shortest current path through the semiconducting region between the source and drain electrodes exceeds the shortest physical distance between the source and drain electrodes (see Fig. 6, insulating region **33**, current path between source **31** and drain **29** must be larger than the physical separation distance between source **31** and drain **29**);

wherein the shortest current path through the semiconductor region between the source and drain electrodes is defined other than by etching the semiconductor region between the source and drain electrodes (see Fig. 4, no etching performed).

Claim Rejections - 35 USC § 103

6. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

7. **Claims 1, 3, 4, 9-14, 16-18, 21, 23, 26, and 29** rejected under 35 U.S.C. 103(a) as being unpatentable over Gu et al.

With regards to **claim 1**, Gu et al. teaches a thin film transistor electronic switching device, comprising:

a source electrode and a drain electrode (see Fig. 6, source **31**. drain **29**);

a semiconducting region in contact with and extending between the source and drain electrodes (see Fig. 6, semiconducting region **23**);

a gate electrode disposed for influencing the transconductance of at least part of the semiconducting region (see Fig. 6, gate electrode **17**, inherent that the gate electrode will influence transconductance since drain current and the gate electrode voltage will change during operation of the device, $g_m = dI / dE$, where dI = change in drain current and dE = change in gate voltage); and

an insulating region located between the source and drain electrodes and configured so that the length of the shortest current path through the semiconducting region between the source and drain electrodes is greater than the shortest physical distance between the source and drain electrodes (see Fig. 6, insulating region **33**, current path between source **31** and drain **29** must be larger than the physical separation distance between source **31** and drain **29**).

Gu et al., however, does not teach shortest current path through the semiconductor region between the source and drain to be greater than 1.05 times the shortest physical distance between the source and drain.

In the same field of endeavor, given the teaching of the references, it would have been obvious to determine the optimum shortest current path (see *In re Aller, Lacey, and Hall* (10 USPQ 233-237). It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical (se *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ 2d 1934,1936 (Fed. Cir. 1990)).

With regards to **claim 3**, Gu et al. teaches a device as claimed in **claim 1**, wherein the shortest current path through the semiconducting region lies closer to the gate electrode than to all paths of the shortest physical distance between the source and drain electrodes (see Fig. 1a, current path between source **31** and drain **29** will be closer to the gate electrode than the physical distance between any point of source **31** and any point of drain **29**).

With regards to **claim 4**, Gu et al. teaches a device as claimed in **claim 1**, wherein the source and drain electrodes comprise an inorganic metallic conductor (see col. 10, lines 31-32).

With regards to **claim 9**, Gu et al. teaches a device as claimed in **claim 1**, wherein the semiconductor region comprises an inorganic semiconductor or nanowires (see col. 7, lines 46-47).

With regards to **claim 10**, Gu et al. does not teach a device as claimed in **claim 1**, wherein the semiconducting region has a mobility exceeding 10^{-3} cm^2/V.

In the same field of endeavor, given the teaching of the references, it would have been obvious to determine the optimum mobility (see *In re Aller, Lacey, and Hall* (10 USPQ 233-237). It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical (se *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ 2d 1934,1936 (Fed. Cir. 1990)).

With regards to **claim 11**, Gu et al. teaches a device as claimed in **claim 1**, wherein the source and drain electrodes make ohmic contact with the semiconducting region (see Fig. 1a, semiconducting region **23** in contact with source **31** and drain **29**).

With regards to **claim 12**, Gu et al. teaches a device as claimed in **claim 1**, wherein the source and drain electrodes make ohmic contact with the semiconductor

region (see Fig. 6, source **31** and drain **29** make ohmic contact with semiconductor region **23**).

With regards to **claim 13**, Gu et al. teaches a device as claimed in **claim 1**, wherein the device has a layer that comprises the source and drain electrodes and a layer that comprises the semiconductor region (see Fig. 6, semiconductor region **23** is one layer, source **31** and drain **29** from metal layer).

With regards to **claim 14**, Gu et al. teaches a device as claimed in **claim 1**, wherein said insulating region comprises a mesa structure of a dielectric material (see Fig. 6, mesa formed).

With regards to **claim 16**, Gu et al. teaches a device as claimed in **claim 1**, comprising a gate dielectric layer between the gate electrode and the semiconducting region (see Fig. 6, gate dielectric layer **21**).

With regards to **claim 17**, Gu et al. does not teach a device as claimed in **claim 1**, wherein the shortest physical distance between the source and drain electrodes is less than one micrometer.

In the same field of endeavor, given the teaching of the references, it would have been obvious to determine the optimum physical distance (see *In re Aller, Lacey, and Hall* (10 USPQ 233-237). It is not inventive to discover optimum or workable ranges by

routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical (se *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ 2d 1934,1936 (Fed. Cir. 1990)).

With regards to **claim 18**, Gu et al. teaches a method for forming a thin film transistor electronic switching device, the method comprising:

forming a source electrode and a drain electrode (see Fig. 1a, source **31** and drain **29**);

forming a semiconducting region in contact with and extending between the source and drain electrodes (see Fig. 6, semiconductor layer **23**);

forming a gate electrode disposed for influencing the transconductance of at least part of the semiconducting region (see Fig. 6, gate electrode **17**, inherent that the gate electrode will influence transconductance since drain current and the gate electrode voltage will change during operation of the device, $g_m = dI / dE$, where dI = change in drain current and dE = change in gate voltage); and

forming an insulating region located between the source and drain electrodes and configured so that the length of the shortest current path through the semiconducting region between the source and drain electrodes exceeds the shortest physical distance between the source and drain electrodes (see Fig. 6, insulating region

33, current path between source **31** and drain **29** must be larger than the physical separation distance between source **31** and drain **29**).

Gu et al., however, does not teach shortest current path through the semiconductor region between the source and drain to be greater than 1.05 times the shortest physical distance between the source and drain.

In the same field of endeavor, given the teaching of the references, it would have been obvious to determine the optimum shortest current path (see *In re Aller, Lacey, and Hall* (10 USPQ 233-237). It is not inventive to discover optimum or workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical (se *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ 2d 1934,1936 (Fed. Cir. 1990)).

With regards to **claim 21**, Gu et al. teaches the limitations of **claim 18** for the reasons above.

Gu et al., however, does not teach the thickness of the insulating region to be in the rage of 30 to 80 nm.

In the same field of endeavor, given the teaching of the references, it would have been obvious to determine the optimum thickness of the insulating region (see *In re Aller, Lacey, and Hall* (10 USPQ 233-237). It is not inventive to discover optimum or

workable ranges by routine experimentation. Note that the specification contains no disclosure of either the critical nature of the claimed ranges or any unexpected results arising therefrom. Where patentability is said to be based upon particular chosen dimensions or upon another variable recited in a claim, the applicant must show that the chosen dimensions are critical (se *In re Woodruff*, 919 f.2d 1575, 1578, 16 USPQ 2d 1934,1936 (Fed. Cir. 1990)).

With regards to **claim 23**, Gu et al. teaches a method as claimed in **claim 18**, wherein the source and drain electrodes are formed by a continuous film coating technique (see col. 10, lines 31-34, metal layer continuously coated on substrate).

With regards to **claim 26**, Gu et al. teaches a method as claimed in **claim 18**, wherein said insulating region is defined by a lithographic patterning technique (see Fig. 6, insulating region **33** etched to form **35**).

With regards to **claim 29**, Gu et al. teaches a method for forming a thin film transistor electronic switching device, the method comprising:

forming a source electrode and a drain electrode (see Fig. 1a, source **31** and drain **29**);

forming a semiconducting region in contact with and extending between the source and drain electrodes (see Fig. 6, semiconductor layer 2**3**);

forming a gate electrode disposed for influencing the transconductance of at least part of the semiconducting region (see Fig. 6, gate electrode **17**, inherent that the gate electrode will influence transconductance since drain current and the gate electrode voltage will change during operation of the device, $g_m = dI / dE$, where dI = change in drain current and dE = change in gate voltage); and

forming an insulating region located between the source and drain electrodes and configured so that the length of the shortest current path through the semiconducting region between the source and drain electrodes exceeds the shortest physical distance between the source and drain electrodes (see Fig. 6, insulating region **33**, current path between source **31** and drain **29** must be larger than the physical separation distance between source **31** and drain **29**).

wherein said insulating region is formed by depositing an insulating material onto the substrate, wherein the insulating material preferably deposits in the region between the source and drain electrodes, but not on top of the source-drain electrodes (see Fig. 6, insulating material **33** between source and drain, it may be preferable but not REQUIRED), and

wherein said insulating material is deposited from a liquid phase (see Fig. 6, insulating layer **33** made of BCB which comes in precursory liquid form).

1. **Claims 5-7** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gu et al. as applied to **claim 1** above, and further in view of Hirai et al.

With regards to **claim 5**, Gu et al. does not teach a device as claimed in **claim 1**, wherein the source and drain electrodes comprise a conducting polymer.

In the same field of endeavor, Hirai et al. teaches a device as claimed in **claim 1**, wherein the source and drain electrodes comprise a conducting polymer (see ¶77, lines 1-2).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate source and drain electrodes comprised of conducting polymers since it has already been made known and demonstrated by Hirai et al.

With regards to **claim 6**, Gu et al. does not teach a device as claimed in **claim 1**, wherein the semiconductor region comprises a solution processible conjugated polymeric or oligomeric material.

In the same field of endeavor, Hirai et al. teaches a device as claimed in **claim 1**, wherein the semiconducting region comprises a solution processible conjugated polymeric or oligomeric material (see ¶84).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate a semiconductor region to comprise of solution processible conjugated polymeric or oligomeric material since it has already been made known and demonstrated by Hirai et al.

With regards to **claim 7**, Gu et al. does not teach a device as claimed in **claim 1**, wherein the semiconducting region comprises a material of small conjugated molecules with solubilising side chains.

In the same field of endeavor, Hirai et al. teaches a device as claimed in **claim 1**, wherein the semiconducting region comprises a material of small conjugated molecules with solubilizing side chains (see ¶97, lines 1-3,28, functional groups utilized).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate a semiconducting region to comprise of a material of small conjugated molecules with solubilising side chains since it has already been made known and demonstrated by Hirai et al.

2. **Claim 8** is rejected under 35 U.S.C. 103(a) as being unpatentable over Gu et al. as applied to **claim 1** above, and further in view of Kostantinos et al.

With regards to **claim 8**, Gu et al. does not teach a device as claimed in **claim 1**, wherein the semiconducting region comprises organic-inorganic hybrid materials self-assembled from solution.

In the same field of endeavor, Kostantinos et al. teaches a device as claimed in **claim 1**, wherein the semiconducting region comprises organic-inorganic hybrid materials self-assembled from solution (see ¶99, lines 1-2,8-10, Konstantinos et al. is taught by Hirai et al. which actually discloses self-assembly materials, see Konstantinos et al., ¶13, lines 3-6).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate a semiconducting region to comprise organic-inorganic hybrid materials self-assembled from solution since it has already been made known and demonstrated by Kostantinos et al.

3. **Claim 15** is rejected under 35 U.S.C. 103(a) as being unpatentable over Gu et al. as applied to **claim 1** above, and further in view of Han et al.

With regards to **claim 15**, Gu et al. teaches the limitations of **claim 1** for the reasons above.

Gu et al., however, does not teach an insulating region to comprise of an air gap.

In the same field of endeavor, Han et al. teaches how incorporating air gaps will reduce heat transmission along a vertical direction because it has low thermal conductivity (see ¶24, lines 11-12,16-17).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to include an air gap as taught by Han et al. in order to reduce heat transmission along a vertical direction because it has low thermal conductivity.

4. **Claims 19,20,22,24,28** are rejected under 35 U.S.C. 103(a) as being unpatentable over Gu et al. as applied to **claim 18** above, and further in view of Hirai et al.

With regards to **claim 19**, Gu et al. does not teach a method as claimed in **claim 18**, wherein the step of forming the semiconducting region is performed after the step of forming the insulating region, the semiconducting region is deposited from solution in contact with the insulating region and the insulating region is capable of repelling the solution from which the semiconducting region is deposited.

In the same field of endeavor, Hirai et al. teaches a method as claimed in **claim 18**, wherein the step of forming the semiconducting region is performed after the step of forming the insulating region, the semiconducting region is deposited from solution in contact with the insulating region and the insulating region is capable of repelling the solution from which the semiconducting region is deposited (see Fig. 4a, semiconducting region **3** formed after insulating region **4** formed; ¶55, lines 5-13, hydrophilic coating on surface will have capability to repel hydrophobic semiconducting region, e.g. organic).

Therefore, it would have been obvious to a person having ordinary skill at the time the invention was made to for a semiconducting region after forming the insulation region with the insulating region capable of repelling solution since it has already been made known and demonstrated by Hirai et al.

With regards to **claim 20**, Gu et al. teaches a method as claimed in **claim 19**, wherein the insulating region comprises a bulk portion of a first composition and a surface portion of a second composition on to which is deposited the solution from which the semconducting region is deposited (see Fig. 6, insulating region comprised of

BCB (benzocyclobutene) which may have some benzene constituents in bulk region and cyclobutene on surface portion or vice versa).

Gu et al., however, does not teach the surface portion being capable of repelling solution.

In the same field of endeavor, Hirai et al. teaches that the surface portion is capable of repelling solution (see ¶55, lines 5-13, hydrophilic coating on surface will have capability to repel hydrophobic semiconducting region, e.g. organic).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to coat the surface portion of the insulating layer with a hydrophilic coating since it will repel hydrophobic solutions during processing and since it has already been made known and demonstrated by Hirai et al.

With regards to **claim 22**, Gu et al. does not teach a method as claimed in **claim 18**, wherein the source and drain electrodes are formed by inkjet printing.

In the same field of endeavor, Hirai et al. teaches a method as claimed in **claim 18**, wherein the source and drain electrodes are formed by inkjet printing (see ¶76, lines 4-13).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to produce source and drain electrodes by inkjet printing since it has already been made known and demonstrated by Hirai et al.

With regards to **claim 24**, Gu et al. does not teach a method as claimed in **claim 18**, wherein one or more components of the device are deposited by vacuum deposition and patterned by photolithography.

In the same field of endeavor, Hirai et al. teaches a method as claimed in **claim 18**, wherein one or more components of the device are deposited by vacuum deposition and patterned by photolithography (see ¶48, gate electrode formed by vacuum evaporation).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to produce one or more components of the device by vacuum deposition and patterned by photolithography since it has already been made known and demonstrated by Hirai et al.

With regards to **claim 28**, Gu et al. teaches a method as claimed in **claim 18**, wherein said insulating region is formed by depositing an insulating material on the substrate, wherein the insulating material preferably deposits in the region between the source and drain electrodes (see Fig. 1a, insulating region **33** between source **31** and drain **29**).

Gu et al., however, does not teach insulating layer to not be on top of electrodes.

In the same field of endeavor, Hirai et al. teaches an insulating material that is not present on top of source and drain electrodes (see Fig. 1a).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate an insulating layer that would not

cover the source and drain electrodes since it has already been made known and demonstrated by Hirai et al.

5. **Claim 25** is rejected under 35 U.S.C. 103(a) as being unpatentable over Gu et al. as applied to **claim 18** above, and further in view of Berger et al.

With regards to **claim 25**, Gu et al. teaches the limitations of **claim 18** for the reasons above.

Gu et al., however, does not teach forming one or more components of the device using electron beam lithography.

In the same field of endeavor, Berger et al. teaches how electron beam lithography offers high resolution, high throughput, and good overlay and registration characteristics (see Abstract, lines 1-3).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to utilize electron-beam lithography to form one ore more components of the device since electron-beam lithography offers high resolution, high throughput, and good overlay and registration characteristics.

6. **Claim 27** is rejected under 35 U.S.C. 103(a) as being unpatentable over Gu et al. as applied to **claim 18** above, and further in view of Grewell et al.

With regards to **claim 27**, Gu et al. teaches the limitations of **claim 18** for the reasons above.

Gu et al., however, does not teach using embossing techniques to forming the insulating region.

In the same field of endeavor, Grewell et al. teaches how embossing techniques are utilized since they have the capability to produce features 10 micrometers in width or even in sub-micron range (see Introduction, lines 1-9).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to use embossing techniques to forming the insulation region because embossing techniques have the capability to produce features in the sub-micron range as taught by Grewell et al.

7. **Claim 30** rejected under 35 U.S.C. 103(a) as being unpatentable over Gu et al. as applied to **claim 28** above, and further in view of Hirai et al.

With regards to **claim 30**, Gu et al. does not teach a method as claimed in **claim 28**, wherein said insulating material is deposited from a vapor phase.

In the same field of endeavor, Hirai et al. teaches a method as claimed in **claim 28**, wherein said insulating material is deposited from a liquid phase (see ¶55, lines 1-4).

Therefore, it would have been obvious to a person having ordinary skill in the art at the time the invention was made to deposit an insulating material from a vapor phase since it has already been made known and demonstrated by Hirai et al.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAE LEE whose telephone number is (571)270-1224. The examiner can normally be reached on Monday - Friday, 7:30 a.m. - 5:00 p.m. EST.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Drew Richards can be reached on 571-272-1736. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

/Jae Lee/
Examiner, Art Unit 2895

/Fernando L. Toledo/
Primary Examiner, Art Unit 2895

JML